flows between the source electrode and the drain electrode through the source region and the drift layer by controlling a voltage applied to the gate electrode.

[0013] In the present SiC semiconductor device, the deep layer is formed along a direction approximately perpendicular to a longitudinal direction of the trench. Thus, a misalignment of a mask for forming the trench and a mask for forming the deep layer does not affect a property of the SiC semiconductor device. Thereby, a variation of a production property can be reduced and a yield can be improved.

[0014] An SiC semiconductor device according to a second aspect of the present invention includes a substrate, a drift layer, a trench, a base region, a source region, a gate insulating layer, a gate electrode, a source electrode, a drain electrode, and a deep layer. The substrate is made of silicon carbide and has one of a first conductivity type and a second conductivity type. The substrate has first and second opposing surfaces. The drift layer is located on the first surface of the substrate. The drift layer is made of silicon carbide. The drift layer has the first conductivity type and has an impurity concentration less than an impurity concentration of the substrate. The trench is provided from a surface of the drift layer. The base region sandwiches the trench so as to be in contact with a sidewall of the trench. The base region is made of silicon carbide and has the second conductivity type. The source region is located on the base region and sandwiches the trench. The source region is in contact with the sidewall of the trench. The source region is made of silicon carbide. The source region has the first conductive type and has an impurity concentration greater than the impurity concentration of the drift layer. The gate insulating layer is located on a surface of the trench. The gate electrode is located on the gate insulating layer in the trench. The source electrode is electrically coupled with the source region and the base region. The drain electrode is located on the second surface of the substrate. The deep layer is located under the base region and extends to a depth deeper than the trench. The deep layer is formed along an approximately normal direction to the sidewall of the trench. The deep layer has the second conductivity type. An inversion channel is provided at a surface portion of the base region located on the sidewall of the trench and electric current flows between the source electrode and the drain electrode through the source region and the drift layer by controlling a voltage applied to the gate electrode.

[0015] In the present SiC semiconductor device, the deep layer is formed along a direction approximately perpendicular to a longitudinal direction of the trench. Thus, a misalignment of a mask for forming the trench and a mask for forming the deep layer does not affect a property of the SiC semiconductor device. Thereby, a variation of a production property can be reduced and a yield can be improved.

[0016] An SiC semiconductor device according to a third aspect of the present invention includes a substrate, a drift layer, a base region, a source region, a trench, a gate insulating layer, a gate electrode, a source electrode, a drain electrode, a deep layer, and a body layer. The substrate is made of silicon carbide and has one of a first conductivity type and a second conductivity type. The substrate has first and second opposing surfaces. The drift layer is located on the first surface of the substrate. The drift layer is made of silicon carbide. The drift layer has the first conductivity type and has an impurity concentration less than an impurity concentration of the substrate. The base region is located on the drift layer. The base region is made of silicon carbide and has the second conductivity type. The source region is located on the base region. The source region is made of silicon carbide. The source region has the first conductive type and has an impurity concentration greater than the impurity concentration of the drift layer. The trench extends to a depth deeper than the source region and the base region and reaches the drift layer. The trench is sandwiched by each of the base region and the source region. The trench is provided along a first direction. The gate insulating layer is located on a surface of the trench. The gate electrode is located on the gate insulating layer in the trench. The source electrode is electrically coupled with the source region and the base region. The drain electrode is located on the second surface of the substrate. The deep layer is located under the base region and extends to a depth deeper than the trench. The deep layer is formed in parallel with a planer direction of the substrate along a second direction crossing the first direction. The deep layer has the second conductivity type. The body layer has a predetermined distance from a sidewall of the trench. The body layer is located at a portion deeper than the source region. The body layer has the second conductivity type and has an impurity concentration greater than the impurity concentration of the base region. A inversion channel is provided at a surface portion of the base region located on the sidewall of the trench and electric current flows between the source electrode and the drain electrode through the source region and the drift layer by controlling a voltage applied to the gate electrode.

[0017] In the present SiC semiconductor device, an on-resistance can be reduced and a breakdown voltage can be increased due to the body layer having the impurity concentration greater than the impurity concentration of the base region.

[0018] An SiC semiconductor device according to a fourth aspect of the present invention includes a substrate, a drift layer, a base region, a source region, a plurality of trenches, a gate insulating layer, a gate electrode, a source electrode, a drain electrode, a deep layer, and a peripheral high-voltage part. The substrate is made of silicon carbide and has one of a first conductivity type and a second conductivity type. The substrate has first and second opposing surfaces. The drift layer is located on the first surface of the substrate. The drift layer is made of silicon carbide. The drift layer has the first conductivity type and has an impurity concentration less than an impurity concentration of the substrate. The drift layer has a cell section and a peripheral section surrounding the cell section. The base region is located on the cell section of the drift layer. The base region is made of silicon carbide and has the second conductivity type. The source region is located on the base region. The source region is made of silicon carbide. The source region has the first conductive type and has an impurity concentration greater than the impurity concentration of the drift layer. The trenches extend to a depth deeper than the source region and the base region and reach the drift layer. The trenches are arranged in a stripe pattern. Each of the trenches is sandwiched by each of the base region and the source region. Each of the trenches is provided along a first direction. The gate insulating layer is located on a surface of each of the trenches. The gate electrode is located on the gate insulating layer in each of the trenches. The source electrode is electrically coupled with the source region and the base region. The drain electrode is located on the second surface of the substrate. The deep layer is located under the base region and extends to a depth deeper than the trenches. The deep layer has the second conductivity type. The deep payer has a